NONCONFIDENTIAL

2010-1302

IN THE UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

FAST MEMORY ERASE, LLC,
Plaintiff-Appellant,

v.

INTEL CORPORATION, NUMONYX B.V., NUMONYX, INC., SONY ERICSSON MOBILE COMMUNICATIONS AB, SONY ERICSSON MOBILE COMMUNICATIONS (USA), INC. and APPLE INC.,
Defendants-Appellees,

and

MOTOROLA, INC.,
Defendant-Appellee.

Appeal from the U.S. District Court for the Northern District of Texas in Case No. 10-CV-0481, Hon. Barbara M.G. Lynn

BRIEF OF APPELLEES INTEL CORPORATION ET AL.

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CERTIFICATE OF INTEREST

Counsel for Appellees Intel Corporation, Numonyx B.V., Numonyx, Inc., Sony Ericsson Mobile Communications AB, Sony Ericsson Mobile Communications (USA), Inc., and Apple Inc. certify the following:

1. The full name of every party or amicus represented by me is: Intel Corporation, Numonyx B.V., Numonyx, Inc., Sony Ericsson Mobile Communications AB, Sony Ericsson Mobile Communications (USA), Inc., and Apple Inc.

2. The name of the real party in interest (if the party named in the caption is not the real party in interest) represented by me: None

3. All parent corporations and any publicly held companies that own 10 percent or more of the stock of the party or amicus curiae represented by me are:

   Intel Corporation: None

   Apple Inc.: None

   Numonyx, Inc. and Numonyx, B.V. were acquired by Micron Technologies, Inc. on May 7, 2010.

   Sony Ericsson Mobile Communications (USA), Inc. is a wholly owned subsidiary of Sony Ericsson Mobile Communications AG. Sony Corporation and Telefonaktiebolaget LM Ericsson each own more than 10% of Sony Ericsson Mobile Communications AB.

4. The names of all law firms and the partners or associates that appeared for the party or amicus now represented by me in the trial court or agency or are expected to appear in this court are:

Chris R. Ottenweller
E. Joshua Rosenkranz
Craig R. Kaufman
Mark S. Davies
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Stacy Margolies
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Dated: February 3, 2011

Mark S. Davies

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Material has been deleted from pages 14-15 and 41-42 of the non-confidential brief of Appellees Intel Corporation et al. This material was designated confidential by FME pursuant to the Protective Order entered on December 22, 2008.

TABLE OF AUTHORITIES

FEDERAL CASES

FEDERAL STATUTES

FEDERAL RULES

STATEMENT OF RELATED CASES

No appeal in or from the same civil action was previously before this Court or any other appellate court.

Fast Memory Erase LLC v. Spansion, Civil Action No. 3:08-cv-0977, and *Fast Memory Erase LLC v. Spansion,* Civil Action No. 3:09-cv-00653, are currently stayed in the U.S. District Court for the Northern District of Texas. The outcome of this appeal will not directly affect the stayed cases because those cases involve a different patent and there has been no claim construction in those cases.

INTRODUCTION

Our age of digital gadgetry rests on the capacity of electronic devices to retain information after the power goes out. A popular form of nonvolatile memory, which consumers use every day in such products as cell phones, cameras, digital music players and USB drives, is "flash memory." Not only does flash memory retain information when the power is turned off, it can be erased and programmed with new information, making it useful in storing files that change frequently. There are two principal designs for erasing a flash memory device: source erase and channel erase. Each design necessarily requires a different physical structure.

The patent asserted by Fast Memory Erase, LLC ("FME"), which it acquired from a failed semiconductor company, is focused solely on source erase devices. Yet FME is attempting to expand the patent beyond its obvious boundaries to cover Defendants' channel erase devices. The district court properly rejected that effort. The court diligently reviewed the asserted claim, specification and prosecution history and came to the "inescapable conclusion" that the claim covers

only source erase devices. That conclusion is supported by overwhelming evidence:

- The patent specification in multiple places describes "the present invention" as a memory device with reduced levels of leakage "during source erase."
- Every embodiment described in the patent is a memory device designed to perform source erase.
- The patent criticizes the leading alternative – channel erase devices – as too complicated and expensive.
- The only problem the patent purports to solve is source leakage "during source erase."
- Nothing in the patent specification even hints at an invention covering a channel erase device.

FME's opening brief does nothing to cast doubt on the district court's decision. FME principally relies on a rhetorical sleight of hand. FME argues that the district court's construction imposed a "method" or "use" limitation on an apparatus claim by limiting the claim to source erase devices. But FME's argument confuses *uses* with *design features*. Source erase and channel erase are design alternatives. As the patent

specification explains, a flash memory device that performs channel erase is designed differently than a flash memory device that performs source erase. This case involves design choices, not limits on uses that can be made of the patented device.

FME cannot claim more under the patent than what the inventor actually invented and disclosed to the public. The district court's construction of the asserted claim placed the proper boundaries on the invention. The district court properly concluded that there is no suggestion whatsoever that the purported invention covers channel erase devices.

Because there is no dispute that Defendants' products are channel erase products, FME conceded that it could not prove infringement. This Court should affirm the judgment of non-infringement.

STATEMENT OF THE ISSUE

The title of U.S. Patent No. 6,303,959 ("the '959 patent") refers to "source erase," the specification describes the "invention" as a "source erase" device, the prior art discussion is focused on improving "source erase" devices and critiques "channel erase" devices and all embodiments are "source erase" devices. Claim 1 refers to a semiconductor device with two doped regions whereby "source leakage," a recognized problem of source erase devices, is reduced. Did the district court properly construe claim 1 of the '959 patent to cover only source erase memory devices?

STATEMENT OF THE CASE

FME is owned by the licensing company Acacia Research Corporation and acquired the patent in suit in 2007 from Alliance Semiconductor, a failed semiconductor manufacturer. FME sued Intel Corporation, Numonyx B.V. and Numonyx Inc., Sony Ericsson Mobile Communications AB and Sony Ericsson Mobile Communications (USA), Inc., and Apple Inc., accusing them of infringing the '959 patent.[1] The district court concluded that a person skilled in the art "would clearly understand" that the claimed invention was a source erase flash memory device. Because the accused products are channel erase flash devices and not source erase devices, FME stipulated to noninfringement after the district court's claim construction ruling.

[1] FME also filed suit based on U.S. Patent No. 6,236,608 ("the '608 patent"), another patent acquired from Alliance. The '608 patent is in reexamination. The district court has stayed all proceedings related to the '608 patent. The products at issue in this appeal are not accused of infringing the '608 patent.

STATEMENT OF FACTS

This is a case about flash memory devices and the design choice that dictates how the devices erase information.[2] Flash memory is widely used to store data in electronic devices, such as cell phones, audio players and digital cameras. A153 (col. 1, ll. 46-49); A2; SVA Ch. 1.[3] Flash memory devices store data as digital 1s or 0s by storing electrons in the "floating gate" of a memory device. SVA Ch. 2.8-2.10. Flash memory can be programmed, erased and reprogrammed multiple times, making it suitable for storing data likely to be changed. SVA Ch. 2.11.

As the patent at issue points out, there are two different techniques and corresponding structures for erasing a flash memory cell —source erase and channel erase. A153 (col. 1, ll. 50-65). The specification explains that these techniques are design choices, implemented through different structures. A flash memory cell

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[2] The particular type of flash memory at issue is referred to as NOR flash memory. "NOR" refers to "Not OR" logic gates.

[3] "SVA" refers to the Supplemental Video Recording Media Appendix, which includes the technology tutorial submitted by Intel et al. to the district court (dkt. no. 258) and filed with this Court pursuant to FED. CIR. R. 30(j). SVA Chs. 1-9.

designed to perform channel erase requires a certain structure described in the specification as "source isolation by the triple well process." *Id.* (col. 1, ll. 56-58). In contrast, a source erase device does not require this structure, which the specification describes as complicated and expensive. *Id.* (col. 1, ll. 50-65) ("Since source erase does not require source isolation by the triple well process it is simpler and less expensive to implement than channel erase.").[4]

Source erase and channel erase are threshold design choices. If a manufacturer elects to design and build a channel erase device, it must adopt the triple well structure referred to in the specification. *Id.* (col. 1, ll. 56-58). A channel erase device cannot erase data using the source erase technique. A7505. Once the design decision is made, the device is fabricated to implement that design choice and only that design choice. A7505; A4807-4808 (504:24-505:12); SVA Ch. 5.

A. Source Erase Devices

The basic physical structure of a flash memory device designed to perform source erase is illustrated below.

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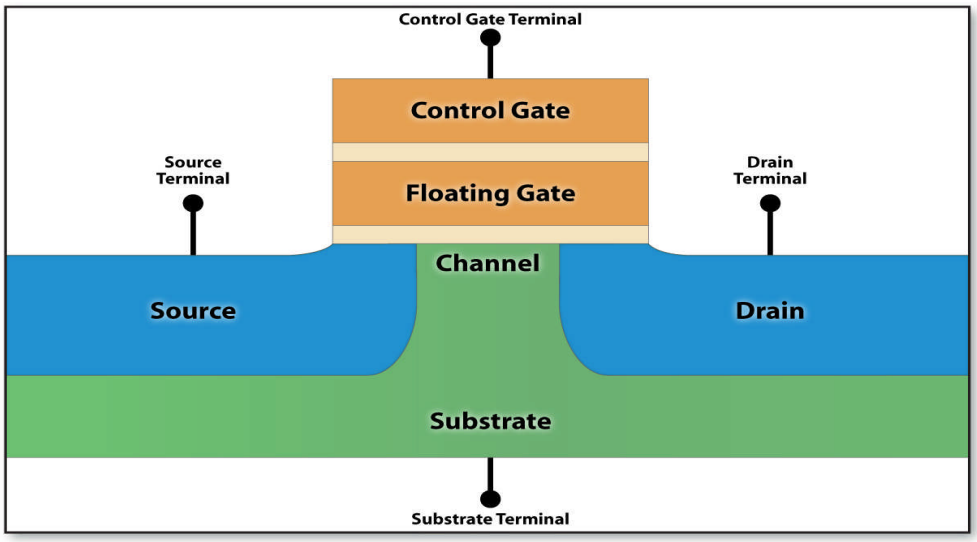
[4] FME refers (at 8) to "hybrid source-channel erase," but the '959 patent refers only to source erase and channel erase. The patent does not discuss "hybrid source-channel erase."



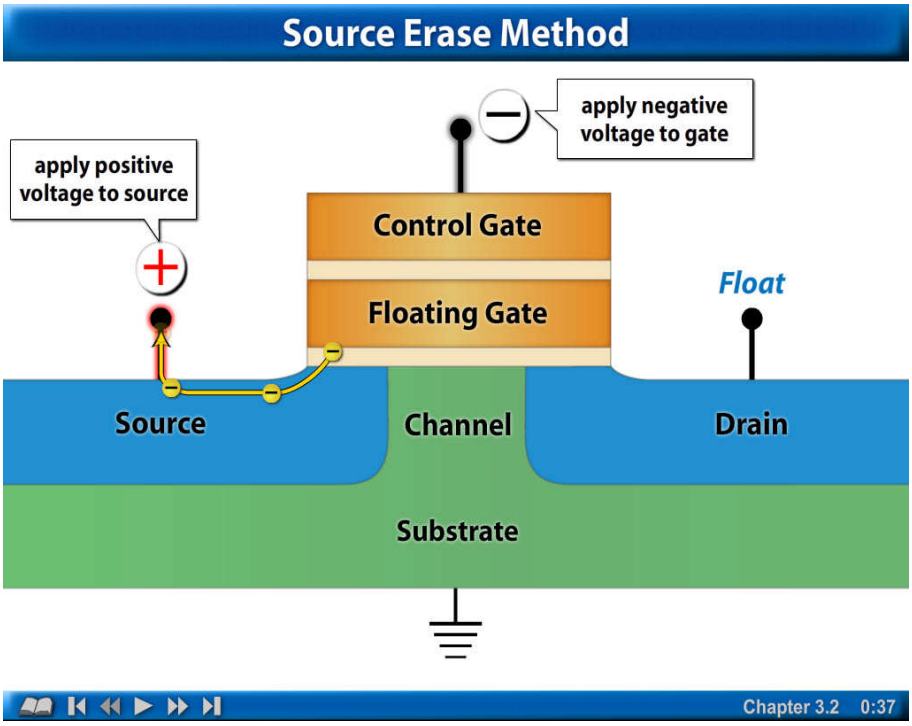
A4570. *See also* SVA Ch. 2.

The "control gate" and "floating gate" (depicted in orange) form what is referred to as a "stacked gate." A4571 at ¶ 11; SVA Ch. 2.7. Data is stored on the device by storing electrons on the floating gate. SVA Ch. 2.8. In a process referred to as "programming," electrons are added to the floating gate. SVA Chs. 2.8-2.9. If the gate has added electrons a "1" may be represented and if the gate does not have added electrons then a "0" may be represented. SVA Ch. 2.10. In this fashion, the device stores digital information.

The device is erased by removing electrons from the floating gate. A3966; SVA Ch. 2.11. This generally is achieved by applying different voltages to different parts of the device. A153 (col. 1, ll. 50-62). As shown above, a flash memory of the type described in the '959 patent

has a "source" and a "drain" (both in blue) that are formed in the semiconductor substrate by adding "dopants." SVA Ch. 2.5. A dopant is an impurity added to the substrate that alters its electrical conductivity. A14; A4583 at ¶ 37; SVA Ch. 8. The "channel" is the part of the substrate (green) between the source and drain. SVA Ch. 2.6. A separate "terminal" or metal line (black) directly connects each of the various individual components of the memory device to power circuitry that generates the necessary voltages to operate the device. *See, e.g.,* A3966. These terminals can be used to provide voltages to the source, drain and substrate regions. A4571.

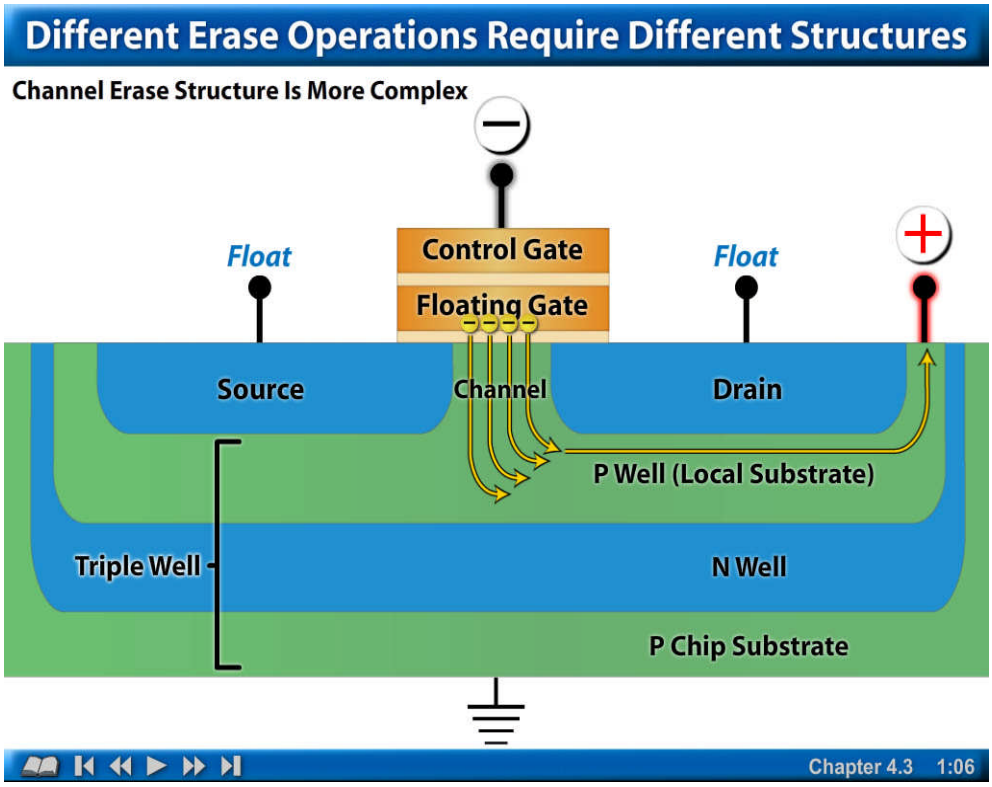
During source erase, a negative voltage is applied to the control gate and a positive voltage is applied to the source. A153 (col. 1, ll. 59-62). This drives the electrons from the floating gate into and *through* the source—thus the expression "source erase." A3966. This is illustrated by the yellow line below:



See A4577-4578 at ¶ 22; SVA Ch. 3.

B. Channel Erase Devices

As the patent at issue explains, a channel erase device "requires source isolation by the triple well process." A153 (col. 1, ll. 56-59). This structure is illustrated below:



SVA Ch. 4.

Channel erase devices are erased by applying a negative voltage to the control gate and a positive voltage to the channel (P Well) terminal. A153 (col. 1, ll. 51-55); SVA Ch. 4.1-4.2. This drives the electrons into the channel. A153 (col. 1, ll., 55-56); A4592 at ¶ 58; SVA Ch. 4.1-4.2. This flow is shown in yellow in the diagram above. In a channel erase device, the electrons generally do not flow through the source. A4820 (60:24-61:10); A3966. And even if some electrons might flow through the source, no electrons in a channel erase device ever flow out through the source terminal. A4820 (60:24-61:10). Instead, the

electrons are drawn out of the floating gate and off through the channel and P Well. *Id.*; A3966.

In contrast to source erase devices, channel erase devices are built with additional doped layers in the substrate, thus forming the "triple well" the '959 patent refers to. A153 (col. 1, ll. 56-58); A3966. In the illustration above, the additional doped layers that form the "triple well" structure are the P Well, N Well and P Chip Substrate. A3964; A3966; SVA Ch. 4. These additional doped layers permit selective erasing of memory cells by isolating the voltage applied to the P Well from the substrate. A3966. Thus, when a positive voltage is applied to the P Well to erase a selected memory cell, the N Well layer isolates the positive voltage from the P Chip Substrate and prevents unintended erasing of other memory cells. *Id.*

Because the source area plays no role in channel erase, the channel erase device has a smaller source region under the gate than a source erase device. A3967. As a result, a channel erase device "can be reduced beyond the minimum size limit for source erase . . . ." A3967 (col. 3, ll. 62-67). Channel erase devices permit fabrication of smaller

memory chips than source erase devices because the size of the memory cell can be reduced as the size of the source is reduced. *See id.*

C. The '959 Patent Discusses The Problem Of Source Leakage During Source Erase

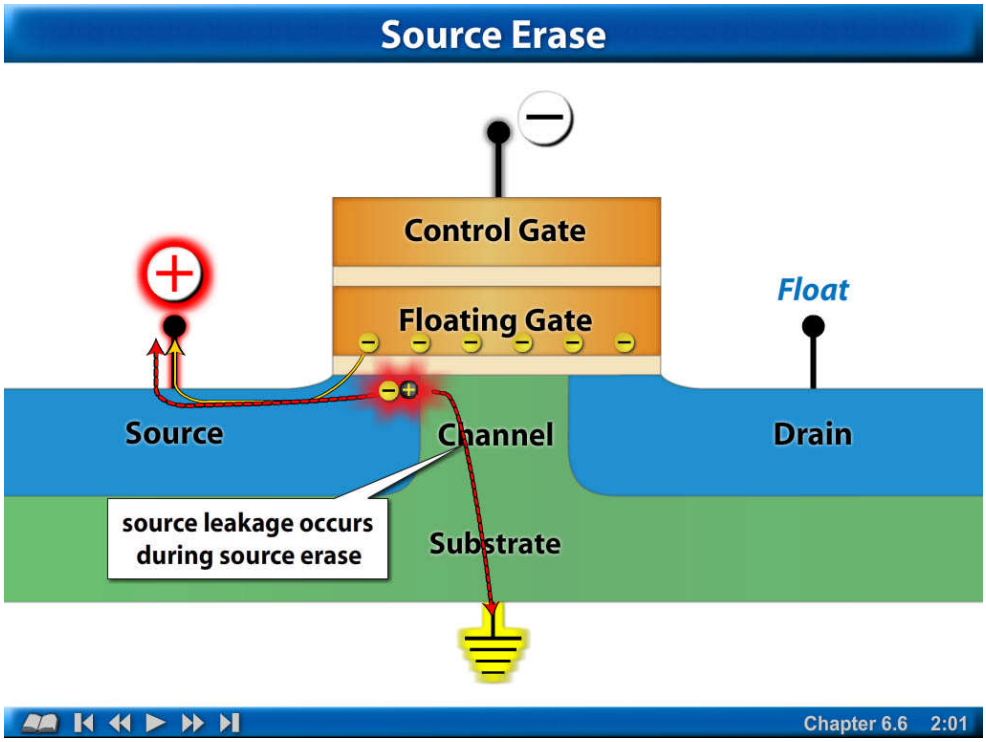
The '959 patent arose from the work of Perumal Ratnam, the sole named inventor on the patent. A137. Dr. Ratnam was attempting to improve the reliability of source erase products at Alliance. A4135 (Dr. Ratnam was "working on source-erase products at Alliance at that time"); A4119 ("[W]e had a problem with the product reliability."); A4135 (Dr. Ratnam was trying to solve the problem of "reduc[ing] source leakage during a source-erase operation"). Dr. Ratnam kept his invention disclosure form, along with other documents related to the '959 patent, in a file entitled "Source Erase Patent Revised Version Process Patent." A4150. Dr. Ratnam referred to the '959 patent as the "source erase patent." A4138 ("Q. So you referred to the '959 patent as the source-erase patent, correct? A. Source-erase patent, yes.").

In the invention disclosure statement, Dr. Ratnam described the problem he was seeking to solve:

[redacted]

A4232 (confidential) (first emphasis added).

Source diode leakage during source erase is shown in the diagram below:



SVA Ch. 6; A153 (col. 1, l. 66 – col. 2, l. 1).

As the picture illustrates, source leakage occurs after a "hole" carrying a positive charge (depicted as a black circle with a yellow +) is

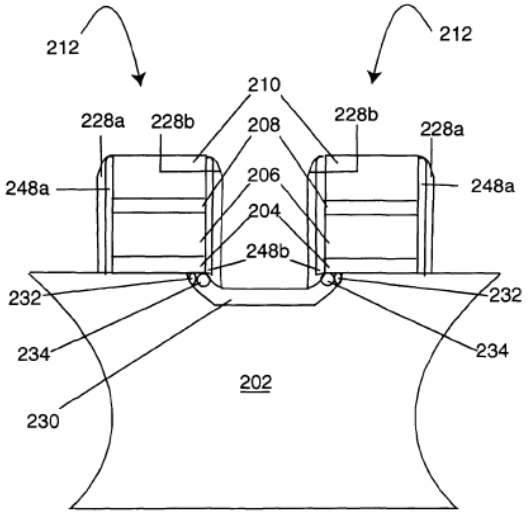
separated from an electron.[5] A4591 at ¶ 52. Although the electron is attracted to and moves towards the positive voltage of the source terminal, the hole is repelled by the positive voltage and moves toward the substrate terminal which is grounded. *Id.* The hole then leaks out through the substrate. *Id.*; A153 (col. 1, l. 66 – col. 2, l. 1).

The '959 patent addresses the problem of "source leakage" during source erase. The specification explains that "leakage is a fundamental problem with source erase." A153 (col. 2, ll. 10-21). It further notes that "[s]ource leakage lengthens the time required to erase" a flash device and "degrades performance." *Id.* (col. 2, ll. 1-2). The specification explains that when the source region is created in a semiconductor device through the self-aligned source ("SAS") etch process, the etching causes a "gouge" and "ragged edge[s]" in the source directly under the edge of the stacked gate. A153-54, A139 (col. 2, l. 52 – col. 3, l. 18, Fig. 2A). This damage leads to increased source leakage during a source erase operation. A153 (col. 2, ll. 22-27, col. 2, l. 52 – col. 3, l. 18).

[5] A "hole" is an empty space in an atom resulting from a missing electron. A hole can readily accept electrons from neighboring atoms. A4584 at ¶ 39.

In proposing a solution to reduce source leakage during source erase, the '959 patent suggests a "differentially doped source region." A153 (col. 1, ll. 12-15). In particular, the specification describes a source region containing two areas with different concentrations of dopant, one greater than the other. A155-56 (col. 6, ll. 59-61, col. 7, ll. 4-14, col. 8, ll. 52-58). The first area, located under the edge of the stacked gate, has the lower dopant concentration. A156 (col. 7, ll. 4-14, col. 8, ll. 52-58). The second area, located at the edge of the source and away from the edge of the stacked gate, has the higher dopant concentration. A156 (col. 7, ll. 4-14, col. 8, ll. 52-58).

The '959 patent illustrates the proposed solution in Figure 8. Region 234 is the "first doped region" and region 232 is the "second doped region" with a higher concentration of dopant. A145; A156 (col. 7, ll. 4-11).

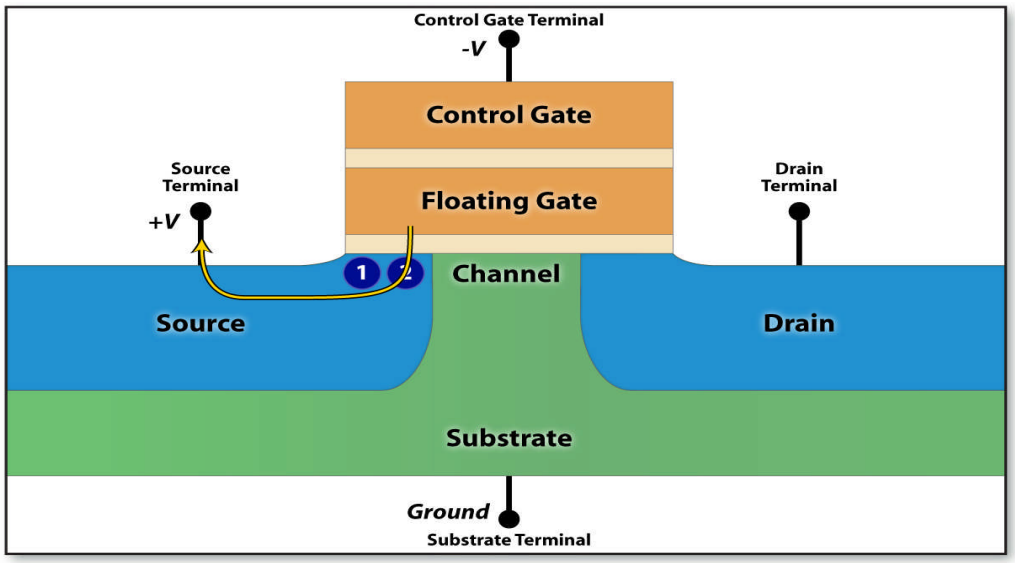


A145 (Fig. 8).

As explained in the '959 patent, this differential in dopant concentration is expected to cause the source erase current to enter the source at a location away from the damage under the edge of the stacked gate. A156 (col. 7, ll. 14-20). Doped region "2," having the greater concentration of dopant, will draw the current into the source away from doped region "1" where the damage exists.[6] *Id.*

[6] Dr. Ratnam never made a chip that verified this theory. A4807 (501:1-6).

This theory is illustrated in the figure below:



A4578; SVA Ch. 7. The dopants in regions 1 and 2 cause the electrons to move on the desired path (the yellow line) through and out the source. A156 (col. 7, ll. 14-20). In theory, having the two doped regions arranged in this manner reduces leakage out through the substrate. A153 (col. 1, ll. 12-15).

D. Prior Proceedings

FME sued Intel and Numonyx, as well as their customers Sony Ericsson and Apple, asserting claim 1 of the '959 patent. A113-15. FME stipulated that "all of the Defendants' products accused of infringing claim 1 of the '959 patent are either . . . flash semiconductor devices that perform channel erase or products incorporating such

devices." A18. FME conceded that these products "do not perform source erase." A7505.

The district court conducted a claim construction hearing. One of the terms in dispute was "source leakage" as used in claim 1:

> A semiconductor device comprising:
>
> a stacked gate provided on a portion of a semiconductor substrate;
>
> a first oxide layer provided on the edge of the stacked gate;
>
> a spacer provided adjacent the first oxide layer; and
>
> a doped source region, the source region having a first doped region disposed under the edge of the stacked gate and a second doped region disposed at the edge of the doped source region under the stacked gate;
>
> wherein the second doped region has a higher concentration of dopant than the first doped region, whereby **source leakage** of the semiconductor device is reduced.

A157 (emphasis added).

Before construing "source leakage," the court addressed a dispute among the experts as to whether source leakage can occur during erase procedures other than source erase. A8-9. The court noted that the '959 patent "specification does not disclaim the possibility of source leakage during channel or other erase procedures." A8. Based on an

article written by FME's expert, Dr. David Liu, the court observed that "source leakage during channel erase is seemingly possible." A9. But the court added that this was not the fundamental issue of claim construction: "Although source leakage during channel erase is seemingly possible, that does not end the inquiry. The claims of a patent cannot be 'of broader scope than the invention that is set forth in the specification.'" A9 (quoting *On Demand Machine Corp. v. Ingram Indus., Inc.*, 442 F.3d 1331, 1340 (Fed. Cir. 2006)).

Next, the district court construed "source leakage" to mean "leakage from the source terminal to the substrate terminal that occurs during source erase." A11. In so doing, the court relied on this Court's settled precedent on claim construction. The court gave four reinforcing rationales for its claim construction:

(1) "While **Defendants cite no fewer than six statements in the specification describing the invention as limiting leakage during source erase**, Plaintiff Fast Memory points to no language in the specification which discusses the benefits of the patent in other erase procedures."

(2) "In fact, the patent distinguishes channel erase as a 'different method' from source erase, and **the specification critiques channel erase for requiring source isolation by the triple well process**, which is complicated and expensive. In contrast, the **specification extols the benefits of source erase**, which is 'simpler and less expensive to implement than channel erase.'"

(3) "**All of the embodiments apply to source erase**."

(4) "The specification addresses the **problem of leakage to the substrate**, not to other parts of the cell."

A9-10 (record citations omitted) (emphasis added).

Next, the district court addressed and rejected FME's remaining claim construction arguments. FME pointed to the specification's mention of "alternative ways of implementing both the process and apparatus of the present invention," but the court ruled that an "analysis of that statement in context reveals that the inventor was referring to dopant concentrations, not to the patent's applicability to channel erase." A10. FME also argued that the court's construction would limit the '959 patent to one of its preferred embodiments, but the court found that "source erase is not merely a preferred embodiment;

analysis of the specification leads to the 'inescapable conclusion' that the claims address only source erase." A10. *See also* A10 ("the reduction of source leakage during source erase is critical to the invention").

In view of the above, the court concluded: "Reading the claim in light of the specification, a person of ordinary skill in the art would clearly understand that the invention refers to source erase, not to other types of erase procedures." A11. "Thus, the Court construes 'source leakage' as: 'leakage from the source terminal to the substrate terminal that occurs during source erase.'" *Id*.

The district court did not construe the term "semiconductor device" in its claim construction order. A1-16.

Thereafter, FME "concede[d] that it cannot prove infringement by Defendants of Claim 1 of the '959 patent in light of the Court's claim construction." A7504. The Court entered a final judgment of non-infringement. A17-20.

SUMMARY OF THE ARGUMENT

The patented device is a flash memory semiconductor designed to perform source erase. The specification repeatedly describes the "current invention" as a "source erase" device and describes only source erase embodiments, criticizes the leading alternative structure ("channel erase") and describes a solution to the "significant problem with source erase." The very title of the patent highlights its focus on "source erase" devices. The extrinsic evidence, including the inventor's contemporaneous documents, confirms that the '959 patent is about source erase devices. The inventor was aware of source erase devices and channel erase devices, yet made no pretense in his description to the public of claiming any invention covering channel erase devices.

In view of the specification and the claim language, the district court properly applied settled claim construction principles to construe claim 1 to cover only source erase devices. To expand claim 1 to cover channel erase devices, as FME urged, would completely negate the inventor's public disclosure of his invention and contradict a long line of this Court's cases holding that the claims of the patent cannot be of a broader scope than the invention set forth in the specification.

FME's appeal brief invokes claim construction principles with no application to this case. For example, FME argues that the district court's construction of claim 1 "disregards the fundamental difference between method and apparatus claims and impermissibly grafts the limitation of performing a particular type of erase into Claim 1, an apparatus claim." Br. 30. The flaw in FME's argument is the incorrect premise that "source erase and channel erase" are "uses" and that a flash memory device can be "used" to perform either technique. As described in the '959 specification, source erase and channel erase are design options, not uses. The court's construction limiting claim 1 to source erase devices has, as a necessary consequence, limited the claim to devices that erase by a particular method. But that is because the apparatus claimed in the '959 patent has a certain design, not because the district court improperly imported a method limitation into an apparatus claim.

FME also argues that the district court erred in construing the "source leakage" term because the term is used in a "whereby" clause. But claim construction is not about fixating on magical words; the search is for what the inventor claims to have conceived. A reduction in

source leakage is an integral part of the claimed invention. Indeed, FME conceded at the claim construction hearing that the '959 patent would not apply to a device with all of the specified structural limitations if the device results in increased source leakage.

The district court should be affirmed.

STANDARD OF REVIEW

Claim construction is a question of law that this Court reviews *de novo*. *Cybor Corp. v. FAS Techs., Inc.*, 138 F.3d 1448, 1456 (Fed. Cir. 1998).

ARGUMENT

The Patent Act requires a patentee to provide both a specification and a claim. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1311 (Fed. Cir. 2005). The first paragraph of 35 U.S.C. § 112 requires a description of the invention while the second paragraph requires a claim that particularly points out the subject matter of the invention. 415 F.3d at 1311-1312. Although the claim defines the invention, the claim is read "in the context of the entire patent, including the specification." *Id.* at 1313. "It is fundamental that claims are to be construed in the light of the specifications and both are to be read with a view to ascertaining

the invention." *Id.* at 1316 (quoting *United States v. Adams*, 383 U.S. 39, 49 (1966)).

I. THE '959 PATENT DISCLOSES ONLY SOURCE ERASE DEVICES

A. The District Court Properly Relied On The Specification In Construing The Scope Of Claim 1

As the district court properly recognized, statements in the Field of the Invention referring to the "invention" and statements in the Detailed Description of the Preferred Embodiments describing only source erase devices establish that any invention disclosed in the '959 patent is a source erase device.

Numerous cases from this Court teach that claims must be aligned with the invention disclosed in the specification. In *Honeywell International, Inc. v. ITT Industries, Inc.*, 452 F.3d 1312 (Fed. Cir. 2006), for example, the Court construed the claim term "fuel injection system component" to mean a "fuel filter" because the description of the "present invention" referred to a fuel filter four times. *Id.* at 1318. The Court stated: "The public is entitled to take the patentee at his word and the word was that the invention is a fuel filter." *Id.* *Accord Alloc, Inc. v. Int'l Trade Comm'n*, 342 F.3d 1361, 1369 (Fed. Cir. 2003) ("specification describes 'the invention'"); *C.R. Bard, Inc. v. U.S.*

Surgical Corp., 388 F.3d 858, 864 (Fed. Cir. 2004) (holding "statements that describe the invention as a whole . . . are more likely to support a limiting definition of a claim term"); *Microsoft Corp. v. Multi-Tech. Sys., Inc.*, 357 F.3d 1340, 1347-48 (Fed. Cir. 2004) (finding claims limited where specification "repeatedly and consistently describes . . . the claimed inventions" as possessing the feature).[7]

In this case, the Field of the Invention begins by stating that the "present invention relates to flash . . . cells and methods for their construction." A153. The specification then states:

> More particularly, the current invention relates to reducing leakage during source erase of flash . . . cells. More specifically, the present invention provides new process techniques that reduce source leakage during source erase of flash . . . cells. **The current invention also provides novel semiconductor devices with a differentially doped source region that reduces leakage during source erase.**

A153 (col. 1, ll. 8-15) (emphasis added).

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[7] *See also*, *e.g.*, *Research Corp. Techs., Inc. v. Microsoft Corp.*, 627 F.3d 859, 872 (Fed. Cir. 2010) ("references to 'the present invention' strongly suggest that the claimed invention is limited"); *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1308 (Fed. Cir. 2007) ("When a patent thus describes the features of the 'present invention' as a whole, this description limits the scope of the invention."); *Akamai Techs., Inc. v. Limelight Networks, Inc.,* No. 09-1372, 2010 WL 5151337, at *13 (Fed. Cir. Dec. 20, 2010) ("the invention" description limits claims).

Under *Honeywell* and the numerous cases cited above, these three descriptions of the "invention" establish that the disclosed invention is a source erase device. All three of the above quoted sentences refer to the "invention" as a "source erase" memory device or process techniques for making such a device. The first sentence refers to "the current invention" as relating to "reducing source leakage during source erase." The second sentence refers to methods of manufacturing a device that reduces source leakage during "source erase." And the third sentence (in bold) expressly defines the "current invention" as a semiconductor device that "reduces leakage during source erase." To paraphrase *Honeywell*, the public is entitled to take the patentee at his word, and the word was that the invention is a source erase device.

FME's efforts to explain away the "invention" descriptions are unpersuasive. FME suggests that the third sentence "merely discuss[es] different ***uses*** to which the apparatus might be put." Br. 40. But that is not what the patent says: "The current invention also provides novel semiconductor devices with a differentially doped source region that reduces leakage during source erase." A153 (col. 1, ll. 12-

15). The third sentence does not refer to uses of the source erase device; it describes a fundamental design feature of the patented device.

In FME's view, the first two sentences discussing "reducing source leakage during source erase" and "reduced source leakage during source erase" are not relevant because they "address the unelected method claims." Br. 39-40 & n.140. According to FME, the "unelected" claims were for "source erase methods and operations." Br. 40 n.140.

But FME's argument is based on a mischaracterization of the abandoned method claims. The abandoned claims do not describe any source erase process or any other type of erasure process. Instead, the abandoned claims address methods for fabricating a semiconductor device through etching, aligning and implanting the substrate. Here is a sample abandoned method claim:

> 1. A method for reducing the source leakage of a semiconductor device comprising:
>
> providing an etched stacked gate disposed on a semiconductor substrate;
>
> forming a thin oxide layer on the stacked gate;
>
> conducting a self-aligned source etch;
>
> forming a spacer on the thin oxide layer; and
>
> performing a source implant on the semiconductor substrate.

A4416. *See also* A4416-18; A4453 (non-elected method claims canceled).

FME cites *LG Electronics, Inc. v. Bizcom Electronics, Inc.*, 453 F.3d 1364, 1378 (Fed. Cir. 2006) (cited at Br. 40 n.144), where certain specification comments (about a multiple cache embodiment) were not used to construe certain claims (regarding data bus monitoring) because the comments had no bearing, as a technical matter, on the claims at issue. In *LG Electronics,* "the original patent application disclosed two inventions" and the disregarded statements were "not relevant to the invention ultimately claimed." 453 F.3d at 1378. Here, in contrast, all the specification statements are substantively relevant to the invention ultimately claimed.

The district court also appropriately noted that every embodiment discussed in the specification is a source erase device, and no embodiment describes any other erase mechanism. When all the embodiments discussed in a specification include a particular feature, the embodiments discussion supports construing the patent's claims to include that particular feature. For example, in *Alloc*, "all the figures and embodiments disclosed in the asserted patents imply play" or "expressly disclose play" and "[i]ndeed, the patents do not show or

suggest any systems without play." *Alloc,* 342 F.3d at 1370. This Court construed the claims to require play: when the specification "makes clear at various points that the claimed invention is narrower than the claim language might imply, it is entirely permissible and proper to limit the claims." *Id*.

Here, after explaining that the first "embodiment described above possesses a number of advantages over the prior art," the specification states: "The culmative [sic] effect of these aforementioned advantages is to provide **a semiconductor device with reduced levels of leakage during source erase**." A156 (col. 7, ll. 39-41) (emphasis added). Similarly, the specification states that the second "described embodiment has some significant advantages over the prior art . . . . These aforementioned advantages provide a semiconductor device with **reduced levels of leakage during source erase**." A157 (col. 9, ll. 18-30) (emphasis added).

Significantly, the patent does not discuss channel erase devices in any of the embodiments. To be sure, the '959 patent includes "boilerplate" language about alternative embodiments:

> Furthermore, it should be noted that there are alternative ways of implementing both the process and apparatus of the

> present invention. For example, the semiconductor substrate may be a lightly doped n-type silicon wafer. The semiconductor device may then be implanted with a p-type dopant. The source regions adjacent to the stacked gate may have different dopant concentrations than those mentioned in the described embodiments.

A157 (col. 9, ll. 35-43). But the example given of an "alternative" embodiment involves possible adjustment of the dopants. There is no description—or even the suggestion—that the inventor considered channel erase devices an "alternative" embodiment.

Nonetheless, FME places great reliance on the boilerplate language, asserting that the patent was "intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims." Br. at 45 (citing A155 (col. 5, ll. 52-55)). It is self evident that such "spirit and scope of the invention" language cannot materially enlarge the scope of a claimed invention. Otherwise, the notice function of a patent would be seriously undermined. *See generally Warner-Jenkinson Co. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 29 (1997) (emphasizing "definitional and public-notice functions of the statutory claiming requirement"); *McClain v. Ortmayer*, 141 U.S. 419, 424 (1891) ("The object of the patent law in requiring the patentee to 'particularly point out and

distinctly claim the part, improvement or combination which he claims as his invention or discovery,' is not only to secure to him all to which he is entitled, but to apprise the public of what is still open to them.").

Indeed, this Court has effectively rejected the same argument based on "spirit and scope" boilerplate language. In *SciMed Life Systems, Inc. v. Advanced Cardiovascular Systems, Inc.,* 242 F.3d 1337 (Fed. Cir. 2001), the specification described "all embodiments of the present invention" to include a particular structure ("a coaxial lumen structure"). *Id.* at 1339. The specification also stated, "Although the present invention has been described with reference to preferred embodiments, workers skilled in the art will recognize that changes may be made in form and detail without departing from the spirit and scope of the invention." U.S. Patent No. 5,156,594 (col. 14, ll. 29-33).[8] Despite this "spirit and scope" language, this Court limited the claims to the embodiments with the particular structure. This Court did not even address the boilerplate language, suggesting that such language has no material effect on claim construction. *Accord Embs v. Jordan*

[8] *See Hoganas AB v. Dresser Indus., Inc.*, 9 F.3d 948, 954 (Fed. Cir. 1993) (Court may take judicial notice of a publicly accessible U.S. patent pursuant to FED. R. EVID. 201(b)(2)).

Outdoor Enters., Ltd., 617 F. Supp. 2d 680, 693 (S.D. Ohio 2008) (noting that patent included "generic reservation" regarding embodiments, that *SciMed* included a "similar generic reservation" yet limited the claims and holding the reservation did not preclude limiting scope of claim).

B. The District Court Properly Relied On The Specification's Criticism Of Channel Erase Devices

The district court properly relied on the specification's criticism of channel erase devices to support limiting the '959 patent to source erase devices. This Court has repeatedly explained that when a specification critiques an alternative structure, the claims will not be construed to reach that structure. In *Edwards Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322 (Fed. Cir. 2009), for example, the "inventors disclaimed the use of resilient, or self expanding, wires" by disparaging "prior art resilient wires in their 'background art' section of the specification." *Id.* at 1332. The patent stated that resilient wires have a "lack of precise control." *Id.* at 1333. This Court construed all the claims not to reach resilient wires: "Where the general summary or description of the invention describes a feature of the invention . . . and criticizes other products . . . that lack that same feature, this operates as a clear

disavowal of these other products." *Id.* (quoting *AstraZeneca AB v. Mut. Pharm. Co.*, 384 F.3d 1333, 1340 (Fed. Cir. 2004)).

The '959 patent specification includes a text book example of disavowing another product. In discussing the related art, the specification begins by describing the advantages of flash memory devices and notes flash "has become the storage method of choice in many portable consumer devices such as cell phones and hand held personal computers." A153 (col. 1, ll. 46-49). The specification then explains that "[t]wo different methods" are "typically used to erase flash." A153 (col. 1, ll. 50-51). In a distinct paragraph, the specification describes how "channel erase" works: "a positive" voltage is applied to the "substrate" and a "negative" voltage to the "gate" that results in "[e]lectron tunneling from the gate to the substrate [that] erases the memory." A153 (col. 1, ll. 51-56). The patent then states, "Channel erase requires source isolation by the triple well process, which is complicated and expensive." A153 (col. 1, ll. 56-58).

In the next paragraph, the specification compares source erase devices with channel erase devices. "Source erase is similar to [channel] erase except that a positive" voltage is applied to the source

while a negative voltage is applied to the gate. A153 (col. 1, ll. 59-62). The specification then states, "Since source erase does not require source isolation by the triple well process it is simpler and less expensive to implement than channel erase." A153 (col. 1, ll. 63-65).

The district court correctly recognized the criticism of channel erase as limiting the scope of the invention to source erase devices. A10. Just as the discussion of resilient wires lacking precise control supported a construction that excluded resilient wires in *Edwards*, the '959 specification's discussion of the problems of channel erase supports construing the claims not to include channel erase devices.

FME implies (see Br. 31) that the district court found no express disclaimer of channel erase devices. But that is not so. The district court only held that the specification did not "disclaim the possibility of source leakage during channel or other erase procedures." A8. That is a different issue from whether the inventor disclaimed channel erase devices as covered by this invention. Regardless of whether source leakage can potentially occur during channel erase, a point not addressed in the specification, the specification makes clear that the inventor did not view his invention as covering channel erase devices.

FME cites *Epistar Corp. v. International Trade Commission*, 566 F.3d 1321 (Fed. Cir. 2009), in which the purported criticism was a "single, passing reference" to a device as "relatively unsatisfactory." *Id.* at 1336. Here, as discussed above, the discussion and criticism of channel erase in the '959 patent is far more than a single aside.

C. The District Court Properly Relied On The Specification's Discussion Of The Problem Of Source Leakage During Source Erase

As with references to "the invention," descriptions of embodiments and critiques of prior art, this Court routinely points to the problem addressed by the patent as one of the signposts informing correct claim construction. For example, in *Honeywell* the Court found support for its claim construction in the problem that the invention was trying to solve – leakage of fuel from prior art fuel filters. 452 F.3d at 1318. The fact that the solution to leaking fuel filters was an improved fuel filter device reinforced the conclusion that a "fuel injection system component" claim was limited to devices that use fuel filters. *Id.* ("detailed discussion of the prior art problem addressed by the patented invention" supported construction). *Accord*, *e.g.*, *Alloc*, 342 F.3d at

1369-70 (criticism of prior art "floor systems without play" supports construing claims not to reach floor systems without play).

Here, the problem addressed by the patent is leakage in a "source erase" device and thus the patent's claims should be construed to reach only source erase devices. The '959 specification describes the problem addressed by the invention as leakage to the substrate during "source erase" of a flash memory cell. A153 (col. 1, l. 66 – col. 2, l. 2) ("[A] significant problem with source erase of flash EPROM cells is source diode leakage to the substrate during erasure. Source leakage lengthens the time required to erase a flash EPROM and degrades performance."). The patent explains that source leakage can occur when the "edge of the source region under the stacked gate . . . was damaged" during the etching process. A153-154 (col. 2, l. 21 – col. 3, l. 18).

FME relies on *Victor Co. of Japan, Ltd.* where the specification discussed two problems with prior art technology, only one of which the patent purported to solve. *Honeywell Inc. v. Victor Co. of Japan, Ltd.*, 298 F.3d 1317, 1326 (Fed. Cir. 2002). In *Victor Co. of Japan*, the Court reasoned that the "fact that the patentee chose to include language in

claim 1 relating to only one of the two cited prior art problems is persuasive evidence that the claim does not require the solution of both problems." 298 F.3d at 1326. But *Victor Co. of Japan, Ltd.* stands for a proposition inapplicable to this case, namely an invention need not attempt to solve all known problems. That principle is inapplicable here because the '959 patent addresses only one problem—source leakage in source erase devices.

D. Other Evidence Confirms That Any Invention Disclosed In The '959 Patent Is A Source Erase Device

Although the many statements in the specification discussed above are more than sufficient to affirm the district court, there are still additional indications that any invention is a source erase device.

The '959 patent is entitled "Semiconductor Device Having Reduced Source Leakage **During Source Erase**." A153 (emphasis added). The patent examiner had objected to the original title for the application, "Process Technique To Improve the Source Leakage of Flash EPROM Cells During Source Erase." A4446. Since the patentee abandoned its claims directed to process techniques, the title had to change so that it is "clearly indicative of the invention to which the claims are directed." A4446. In response, the inventor amended the

title to be "Semiconductor Device Having Reduced Source Leakage During Source Erase." A4452. Exactly so.

Moreover, the '959 specification equates "source leakage" to "source diode leakage." A153 (col. 1, l. 66 – col. 2, l. 3). The specification explains that source leakage/source diode leakage occurs during source erase. *Id.* (col. 1, l. 66 – col. 2, l. 1) ("However, a significant problem with source erase of flash EPROM cells is source diode leakage to the substrate during erasure."). The '959 specification also confirms that source leakage is leakage from the source to the substrate. *Id.* (col. 2, ll. 12-14) ("Band to band leakage wastes power since some of the diode current is dissipated in the substrate during erasure.").

Inventor testimony confirms that the actual invention is a source erase device. Inventor and expert testimony can "shed useful light" and thereby confirm a proper claim construction. *Phillips*, 415 F.3d at 1317; *see id*. at 1319 ("extrinsic evidence may be useful to the court"). Dr. Ratnam testified he was "trying to solve" the problem of "reduc[ing] source leakage during a source-erase operation." A4135. His invention disclosure statement emphasized that [redacted]

[redacted] A4232 (confidential) (original emphasis). Dr. Ratnam saved documents related to the '959 patent in a file entitled "Source Erase Patent Revised Version Process Patent." A4150. He referred to the '959 patent as the "source erase patent." A4138 ("Q. So you referred to the '959 patent as the source-erase patent, correct? A. Source-erase patent, yes."). Furthermore, as the district court stated, Dr. Liu, FME's expert, "in his declaration, noted that the '959 patent 'addresses the issue of reducing source leakage during erasure of the source of a semiconductor device.'" A11.

* * *

The title of the patent, the "current invention" summary, the two embodiments, the criticism of the leading alternative, the problem under discussion, the very file the inventor stored the material in and even the testimony of the patentee's expert all converge on a single point: the scope of the '959 patent is limited to a source erase device.

II. FME'S REMAINING ARGUMENTS LACK MERIT

A. The District Court Did Not Import A Method Limitation Into Claim 1

FME argues (Br. 28-33) that "[t]he district court's construction of Claim 1 disregards the fundamental difference between method and

apparatus claims and impermissibly grafts the limitation of performing a particular type of erase into Claim 1, an apparatus claim." Br. 30. FME emphasizes that "any semiconductor device manufactured to include the structures of the '959 patent infringes apparatus Claim 1, irrespective of how it is used." Br. 30-31. Similarly, FME asserts it "is entitled to the benefit of all the uses to which the claimed 'novel semiconductor device' can be put." Br. 31.

The fundamental flaw in FME's argument is that it confuses design with use. As discussed above, the method of erasure is a design choice incorporated in the chip during the pre-fabrication design process. *See supra* pp. 4-6. Source erase and channel erase techniques are not "uses" of a semiconductor device.

The district court concluded that claim 1 covers only a particular type of design. But it imposed no limitations on how a device covered by claim 1 might be used. It could be used in digital media players or laptop computers; it could be used to store operating code or ringtones; it could be used in computers or home appliances.

To put the same point more generally, FME's claim construction argument conflates rationale and consequence. The consequence of the

district court's construction is that the '959 patent covers only source erase devices. But that consequence is a direct result of the physical reality that any particular flash memory device only performs one type of erasure. *See supra* pp. 4-6; A7505; A153; A4807-4808 (504:24-505:12); A3966 (describing memory cells "configured to employ channel erase"). It has nothing to do with the claim construction methodology.

Because the district court construed the '959 patent as reaching a particular type of apparatus, the cases relied upon by FME are fully consistent with the district court's construction of the '959 patent. For example, FME quotes (Br. 29-30) from *Paragon Solutions, LLC v. Timex Corp.*, 566 F.3d 1075 (Fed. Cir. 2009). There, the Court recited the familiar principle that "[a]pparatus claims cover what a device *is*, not what a device does." *Id.* at 1090 (quoting *Hewlett-Packard Co. v. Bausch & Lomb, Inc.,* 909 F.2d 1464, 1468 (Fed. Cir. 1990)). This undisputed principle has no bearing here. The '959 patent claims a memory device with a certain structure; the court imposed no limits on how such a device can be used.

B. The District Court Did Not Err In Deciding To Construe "Source Leakage"

In FME's view, the phrase in claim 1 "whereby source leakage of the semiconductor device is reduced" is not a limitation on the scope of the claim. Instead, FME argues that the "whereby" clause should be ignored because it "merely describes a possible use, and, more specifically, an intended benefit of the claimed apparatus." Br. 50. This is wrong.

By its plain terms, the "whereby" clause in claim 1 defines the scope of claim 1. In *Hoffer v. Microsoft Corp.*, 405 F.3d 1326 (Fed. Cir. 2005), relied upon by the district court, this Court articulated an analytical framework for determining when a "whereby" clause should be treated as a claim limitation. *Id.* at 1329. If "the 'whereby' clause states a condition that is material to patentability, *it cannot be ignored* in order to change the substance of the invention." *Id.* (emphasis added); *see also Griffin v. Bertina*, 285 F.3d 1029, 1033 (Fed. Cir. 2002) (no error in "giving limiting effect to the 'wherein' clauses because they relate back to and clarify what is required by the count"). In contrast, a "whereby" clause "is not given weight when it simply expresses the intended result of a process step positively recited." *Hoffer*, 405 F.3d at

1329 (quoting *Minton v. Nat'l Ass'n of Sec. Dealers, Inc.*, 336 F.3d 1373, 1381 (Fed. Cir. 2003)).

The reduction of source leakage is material to patentability. The limitation requires that the second doped region must have a higher concentration of dopant compared to the first doped region. But this difference in concentration must not be some *de minimis* amount.[9] Rather, the concentrations of dopant must be adequate to provide a specific functional result—the reduction of source leakage during source erase.

For at least 40 years, this Court has condoned functional claiming of this type, where a device is defined by "what it does rather than what it is (as evidenced by specific structure or material)." *In re Swinehart*, 439 F.2d 210, 212 (C.C.P.A. 1971); *Microprocessor Enhancement Corp. v. Texas Instruments, Inc.*, 520 F.3d 1367, 1375 (Fed. Cir. 2008) ("Functional language may also be employed to limit the claims without

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[9] The '959 patent discloses exemplary dopant concentrations for the "second doped region" that are two to five times higher than the dopant concentration for the first doped region. A154 (col. 4, ll. 49-53) ("[T]he second doped region has a dopant concentration of $5x10^{19}$ atoms/cm^3 and the first doped region has a dopant concentration of about $1x10^{19}$ atoms/cm^3."); A157, claim 2 (first doped region concentration of $5x10^{19}$ atoms/cm^3 and second doped region concentration of $1x10^{20}$ atoms/cm^3).

using the means-plus-function format."); *Halliburton Energy Servs., Inc. v. M-I LLC*, 514 F.3d 1244, 1255 (Fed. Cir. 2008) (recognizing that "'there is nothing intrinsically wrong with' using functional language in claims") (quoting *In re Swinehart*, 439 F.2d at 212).

FME suggests (at 48) that *Hoffer* does not apply here. In FME's view, *Hoffer* is limited to method claims while here the '959 includes apparatus claims. But *Hoffer* never states that its holding is so constricted, and FME cites no authority or rationale for that novel proposition. The reasoning of *Hoffer* plainly applies here because to ignore the "whereby clause" would impermissibly "change the substance of the invention." 405 F.3d at 1329.

Contrary to FME's contention, in claim 1 the whereby clause does not merely describe a "possible use" of the claimed product. *See* Br. 50. Instead, it describes a required condition of the claimed invention. A device that does **not** have reduced source leakage would not come within the inventor's description of his invention. If the Court were to ignore reduction in source leakage, as FME urges, the invention would be expanded to cover the antithesis of what the inventor described, *i.e.*, a device with increased source leakage.

Even FME did not endorse such an illogical result in the proceedings below. During the claim construction hearing, the district court asked FME's counsel if FME is taking the position that claim 1 would cover a device with the specified "differentially doped" source regions but which has **increased** source leakage:

> The Court: Are you, Mr. Bragalone, going to answer that rhetorical question, yes, that the claim will cover increased source leakage? . . .
>
> Mr. Bragalone: The short answer is no.

A7747 (emphasis added). By conceding that claim 1 does not cover structures with increased source leakage, FME has confirmed that reduced source leakage is a necessary condition of an apparatus covered by claim 1.

C. The District Court Properly Rejected FME's Construction

The district court properly rejected FME's proposed construction of "source leakage," a construction that FME does not reassert on appeal. FME proposed to define source leakage as "an unwanted and slow escape or entrance of particles or material which may be conveyed between the source terminal and ground or other parts." A9. As the district court properly noted, this proposed construction "is not found in

or supported by the intrinsic record." *Id.* The '959 specification defines source leakage as leakage to the substrate, not to "ground or other parts." Moreover, there is no support in the intrinsic record for a description of source leakage as a "slow escape or entrance of particles or material." FME's proposed construction also ignores the multiple references in the specification that source leakage is leakage occurring during source erase. A9-10.

D. The District Court Did Not Construe The Term "Semiconductor Device"

FME devotes 10 pages (Br. 33-43) to disputing a claim construction that the district court never made. The district court did not construe the term "semiconductor device." A1-16. In light of the construction of "source leakage," there was no need to. Giving the game away, FME repeatedly uses the phrase "effectively construed" in describing the court's purported construction of "semiconductor device." Br. 34, 35, 36. There was no "effective" construction of semiconductor device because the construction of "source leakage" resolved the case.

CONCLUSION AND RELIEF SOUGHT

The '959 patent describes a flash memory device that provides reduced source leakage during source erase. The district court properly followed this Court's precedent, examined the specification and the language of the claim and concluded that claim 1 of the '959 patent should be construed to cover flash memory source erase semiconductor devices. The accused products are not source erase devices. The district court's judgment should be affirmed.

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CERTIFICATE OF SERVICE

I hereby certify that on this 3rd day of February 2011, two copies of the confidential and nonconfidential versions of the **Brief of Appellees Intel Corporation Et Al**. were served by Federal Express to the following:

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_____

CERTIFICATE OF COMPLIANCE

Counsel for appellees certifies that the brief contained herein has a proportionally spaced 14-point typeface and contains 8,617 words, based on the "Word Count" feature of Microsoft Word, including footnotes and endnotes. Pursuant to Federal Rule of Appellate Procedure 32(a)(7)(B)(iii) and Federal Circuit Rule 32(b), this word count does not include the words contained in the Certificate of Interest, Certificate of Service, Table of Contents, Table of Authorities, and Statement of Related Cases.

Dated: February 3, 2011

Respectfully submitted,

Mark S. Davies/EG

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DECLARATION OF AUTHORITY

In accordance with Fed. Cir. R. 47.3(d), and 28 U.S.C. § 1746, I, Eric Grunspan, hereby declare under the penalty of perjury that Mark Davies has authorized me to sign the foregoing Certificate of Compliance with the Word Count, on his behalf.

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